DIGITAL LOGIC DESIGN LAB

List of Experiments:
1) Verification of Basic Logic Gates.
2) Implementing all individual gates with Universal Gates NAND & NOR.
3) Design a circuit for the given Canonical form, draw the circuit diagram and verify the De-Morgan laws.
4) Design a Combinational Logic circuit for 4x1 MUX and verify the truth table.
5) Design a Combinational Logic circuit for 1x4 De- MUX and verify the truth table.
6) Verify the *data read* and *data write* operations for the IC 74189.
7) Design a Gray code encoder and interface it to SRAM IC 74189 for write operation display on 7-segment.
8) Design a Gray code De-coder and interface it to SRAM IC 74189 for read operation display it on 7-segment.
9) Construct Half Adder and Full Adder using Half Adder and verify the truth table.
10) Verification of truth tables of the basic Flip- Flops with *Synchronous* and *Asynchronous* modes.
11) Implementation of Master Slave Flip-Flop with J-K Flip- Flop and verify the truth table for *race around* condition.
12) Design a Decade Counter and verify the truth table.
13) Design the Mod 6 counter using D-Flip -Flop.
14) Construct 4-bit ring counter with T-Flip –Flop and verify the truth table.
15) Design a 8 – bit right Shift Register using D-Flip -Flop and verify the truth table.